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Claims

[c1] What is claimed is:

1.A method of forming at least one wire on a substrate, the substrate comprising at least one conductive region, an insulating layer disposed on the substrate, the method comprising:

forming a hard mask layer on a surface of the insulating layer;

forming at least one recess by removing portions of the hard mask layer and portions of the insulating layer;

forming a light blocking layer on a surface of the hard mask layer and the recess, the light blocking layer and the hard mask layer forming a composite layer;

forming a gap filling layer on a surface of the light blocking layer, and the gap filling layer filling up the recess;

forming a photoresist layer on a surface of the gap filling layer;

aligning a photo mask with the recess by utilizing the composite layer as a mask; and

performing an exposure and development process to form at least one pattern above the recess in the photoresist layer.

[c2] 2.The method of claim 1 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

[c3] 3.The method of claim 1 wherein the conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor, and the recess is formed above the conductive region.

[c4] 4.The method of claim 3 wherein the recess exposes the conductive region.

[c5] 5.The method of claim 4 further comprising the following steps after forming the pattern in the photoresist layer:
performing an etching process by utilizing the photoresist layer as a mask to remove portions of the gap filling layer, the light blocking layer, the hard mask layer, and the insulating layer to form at least one trench of at least one dual damascene structure;
removing the photoresist layer;
removing the remaining gap filling layer;
forming a barrier layer on a surface of the light blocking layer and the dual damascene structure;
performing a re-sputter process to expose the conduc-

tive region;

forming a seed layer on a surface of the barrier layer and the exposed conductive layer; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the dual damascene structure.

[c6] 6.The method of claim 3 wherein the recess does not expose the conductive region.

[c7] 7.The method of claim 6 further comprising the following steps after forming the pattern in the photoresist layer:

performing an etching process by utilizing the photoresist layer as a mask to remove portions of the gap filling layer, the light blocking layer, the hard mask layer, and the insulating layer to form at least one via of at least one dual damascene structure;

removing the photoresist layer;

removing the remaining gap filling layer;

forming a barrier layer on a surface of the light blocking layer and the dual damascene structure;

performing a re-sputter process to expose the conductive region;

forming a seed layer on a surface of the barrier layer and the exposed conductive region; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the a dual damascene structure.

[c8] 8.The method of claim 1 wherein the conductive region is an alignment mark, and the recess is formed aside the conductive region.

[c9] 9.The method of claim 8 wherein the composite layer is used to prevent light from reaching to the conductive region when aligning the photo mask with the recess to improve alignment accuracy.

[c10] 10.The method of claim 1 wherein the hard mask layer is a titanium nitride layer (TiN layer).

[c11] 11.The method of claim 10 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å).

[c12] 12.The method of claim 1 wherein the light blocking layer comprises a titanium nitride layer or a tantalum nitride layer (TaN layer).

[c13] 13.The method of claim 12 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å).

[c14] 14.The method of claim 1 wherein the gap filling layer is a bottom anti-reflective coating (BARC) and is formed by a spin coating process.

[c15] 15.A method of forming at least one wire on a substrate, the substrate comprising at least one first conductive re-

gion and at least one second conductive region, an insulating layer disposed on the substrate, the method comprising:

forming a hard mask layer on a surface of the insulating layer;

forming at least one first recess above the first conductive region and at least one recess aside the second conductive region by removing portions of the hard mask layer and portions of the insulating layer;

forming a light blocking layer on a surface of the hard mask layer, the first recess, and the second recess, the light blocking layer and the hard mask layer forming a composite layer;

forming a gap filling layer on a surface of the light blocking layer, and the gap filling layer filling up the first recess and the second recess;

forming a photoresist layer on a surface of the gap filling layer;

aligning a photo mask with the second recess by utilizing the composite layer as a mask; and

performing an exposure and development process to form at least one pattern above the first recess in the photoresist layer.

[c16] 16.The method of claim 15 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator

substrate (SOI substrate).

[c17] 17.The method of claim 15 wherein the first conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

[c18] 18.The method of claim 17 wherein the first recess exposes the first conductive region.

[c19] 19.The method of claim 18 further comprising the following steps after forming the pattern in the photoresist layer:

performing an etching process by utilizing the photoresist layer as a mask to remove portions of the gap filling layer, the light blocking layer, the hard mask layer, and the insulating layer to form at least one trench of at least one dual damascene structure;

removing the photoresist layer;

removing the remaining gap filling layer;

forming a barrier layer on a surface of the light blocking layer and the dual damascene structure;

performing a re-sputter process to expose the first conductive region;

forming a seed layer on a surface of the barrier layer and the exposed first conductive region; and

forming a metal layer on a surface of the seed layer, and

the metal layer filling up the dual damascene structure.

[c20] 20.The method of claim 17 wherein the recess does not expose the first conductive region.

[c21] 21.The method of claim 20 further comprising the following steps after forming the pattern in the photoresist layer:
performing an etching process by utilizing the photoresist layer as a mask to remove portions of the gap filling layer, the light blocking layer, the hard mask layer, and the insulating layer to form at least one via of at least one dual damascene structure;
removing the photoresist layer;
removing the remaining gap filling layer;
forming a barrier layer on a surface of the light blocking layer and the dual damascene structure;
performing a re-sputter process to expose the first conductive region;
forming a seed layer on a surface of the barrier layer and the exposed first conductive region; and
forming a metal layer on a surface of the seed layer, and the metal layer filling up the a dual damascene structure.

[c22] 22.The method of claim 15 wherein the second conductive region is an alignment mark, and the composite layer is used to prevent light from reaching to the sec-

ond conductive region when aligning the photo mask with the second recess to improve alignment accuracy.

[c23] 23.The method of claim 15 wherein the hard mask layer is a titanium nitride layer (TiN layer).

[c24] 24.The method of claim 23 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å)

[c25] 25.The method of claim 15 wherein the light blocking layer comprises a titanium nitride layer or a tantalum nitride layer (TaN layer).

[c26] 26.The method of claim 25 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å).

[c27] 27.The method of claim 15 wherein the gap filling layer is a bottom anti-reflective coating (BARC) and is formed by a spin coating process.

[c28] 28.A method of forming at least one wire on a substrate, the substrate comprising at least one first conductive region and at least one second conductive region, aan insulatinglayer disposed on the substrate, the method comprising:
forming at least one first recess above the first conductive region and at least one recess aside the second conductive region by removing portions of the insulating

layer;

forming a bottom anti-reflective coating (BARC)on a surface of the insulating layer, the first recess, and the second recess, and the bottom anti-reflective ccoating fillingup the first recess;

forming a photoresist layer on a surface of the bottom anti-reflective coating, and the photoresist layer filling up the second recess;

aligning a photo mask with the second recess by utilizing the bottom anti-reflective coating as a mask; and

performing an exposure and development process to form at least one pattern above the first recess in the photoresist layer.

[c29] 29.The method of claim 28 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

[c30] 30.The method of claim 28 wherein the first conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

[c31] 31.The method of claim 30 wherein the first recess exposes the first conductive region.

[c32] 32.The method of claim 31 further comprising the fol-

lowing steps after forming the pattern in the photoresist layer:

performing an etching process by utilizing the photoresist layer as a mask to remove portions of the bottom anti-reflective coating and the insulating layer to form at least one trench of at least one dual damascene structure;

removing the photoresist layer;

removing the remaining bottom anti-reflective coating;

forming a barrier layer on a surface of the insulating layer and the dual damascene structure;

performing a re-sputter process to expose the first conductive region;

forming a seed layer on a surface of the barrier layer and the exposed first conductive region; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up tthe dualdamascene structure.

[c33] 33.The method of claim 30 wherein the recess does not expose the first conductive region.

[c34] 34.The method of claim 33 further comprising the following steps after forming the pattern in the photoresist layer:

performing an etching process by utilizing the photoresist layer as a mask to remove portions of the bottom anti-reflective coating and the insulating layer to form at

least one via of at least one dual damascene structure;
removing the photoresist layer;
removing the remaining bottom anti-reflective coating;
forming a barrier layer on a surface of the insulating layer and the dual damascene structure;
performing a re-sputter process to expose the first conductive region;
forming a seed layer on a surface of the barrier layer and the exposed first conductive region; and
forming a metal layer on a surface of the seed layer, and the metal layer filling up the a dual damascene structure.

[c35] 35.The method of claim 28 wherein the second conductive region is an alignment mark, and the bottom anti-reflective coating is used to prevent light from reaching to the second conductive region when aligning the photo mask with the second recess to improve alignment accuracy.

[c36] 36.The method of claim 28 wherein the bottom anti-reflective coating is a light absorptive coating.

[c37] 37.The method of claim 28 wherein a thickness of the bottom anti-reflective coating is approximately 600~1200 angstroms ((Å

[c38] 38.The method of claim 28 wherein the bottom anti-

reflective coating is composed of organic materials, and the bottom anti-reflective coating is formed by a spin coating process.

[c39] 39.The method of claim 38 wherein the organic materials comprises dyes.